

## GENERAL DESCRIPTION

This chapter gives an overview of the 260-pin SO DDR4 Dual-In-Line memory modules product family and describes its main characteristics.

## FEATURES

- VDD=VDDQ=1.2V +/- 0.06V
- VPP = 2.5V, -125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 85°C
- 64ms, 8192-cycle refresh at 0°C to 85°C
- JEDEC standard 78ball FBGA
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Post package repair (PPR) and soft post package repair (sPPR) modes • JEDEC JESD-79-4 compliant

## Information for Compliant Products

Product Type	Compliance Code	Description
IND-ID4N21SP08X	8GB DDR4-2133 15/15/15	1 Ran, Non-ECC
IND-ID4N24SP08X	8GB DDR4-2400 17/17/17	1 Ran, Non-ECC
IND-ID4N26SP08X	8GB DDR4-2666 19/19/19	1 Ran, Non-ECC
IND-ID4N29SP08X	8GB DDR4-2933 21/21/21	1 Ran, Non-ECC
IND-ID4N32SP08X	8GB DDR4-3200 22/22/22	1 Ran, Non-ECC

## Pinout

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol		
1	V <sub>SS</sub>	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	V <sub>SS</sub>	68	V <sub>SS</sub>	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	V <sub>SS</sub>	135	V <sub>DD</sub>	201	V <sub>SS</sub>	4	DQ4	70	DQ24	136	V <sub>DD</sub>	202	V <sub>SS</sub>
5	V <sub>SS</sub>	71	DQ25	137	CK0_t	203	DQ46	6	V <sub>SS</sub>	72	V <sub>SS</sub>	138	CK1_t/NF	204	DQ47
7	DQ1	73	V <sub>SS</sub>	139	CK0_c	205	V <sub>SS</sub>	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	V <sub>SS</sub>
9	V <sub>SS</sub>	75	DM3_n/ DBI3_n	141	V <sub>DD</sub>	207	DQ42	10	V <sub>SS</sub>	76	DQS3_t	142	V <sub>DD</sub>	208	DQ43
11	DQS0_c	77	V <sub>SS</sub>	143	PARITY	209	V <sub>SS</sub>	12	DM0_n/ DBI0_n	78	V <sub>SS</sub>	144	A0	210	V <sub>SS</sub>
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	V <sub>SS</sub>	80	DQ31	146	A10/AP	212	DQ53
15	V <sub>SS</sub>	81	V <sub>SS</sub>	147	V <sub>DD</sub>	213	V <sub>SS</sub>	16	DQ6	82	V <sub>SS</sub>	148	V <sub>DD</sub>	214	V <sub>SS</sub>
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	V <sub>SS</sub>	84	DQ27	150	BA0	216	DQ48
19	V <sub>SS</sub>	85	V <sub>SS</sub>	151	WE_n/ A14	217	V <sub>SS</sub>	20	DQ2	86	V <sub>SS</sub>	152	RAS_n/ A16	218	V <sub>SS</sub>
21	DQ3	87	CB5/NC	153	V <sub>DD</sub>	219	DQS6_c	22	V <sub>SS</sub>	88	CB4/NC	154	V <sub>DD</sub>	220	DM6_n/ DBI6_n
23	V <sub>SS</sub>	89	V <sub>SS</sub>	155	ODT0	221	DQS6_t	24	DQ12	90	V <sub>SS</sub>	156	CAS_n/ A15	222	V <sub>SS</sub>
25	DQ13	91	CB1/NC	157	CS1_n	223	V <sub>SS</sub>	26	V <sub>SS</sub>	92	CB0/NC	158	A13	224	DQ54
27	V <sub>SS</sub>	93	V <sub>SS</sub>	159	V <sub>DD</sub>	225	DQ55	28	DQ8	94	V <sub>SS</sub>	160	V <sub>DD</sub>	226	V <sub>SS</sub>
29	DQ9	95	DQS8_c	161	ODT1	227	V <sub>SS</sub>	30	V <sub>SS</sub>	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	V <sub>SS</sub>	97	DQS8_t	163	V <sub>DD</sub>	229	DQ51	32	DQS1_c	98	V <sub>SS</sub>	164	V <sub>REFCA</sub>	230	V <sub>SS</sub>
33	DM1_n/ DBI_n	99	V <sub>SS</sub>	165	C1,CS3_n, NC	231	V <sub>SS</sub>	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	V <sub>SS</sub>	101	CB2/NC	167	V <sub>SS</sub>	233	DQ61	36	V <sub>SS</sub>	102	V <sub>SS</sub>	168	V <sub>SS</sub>	234	V <sub>SS</sub>
37	DQ15	103	V <sub>SS</sub>	169	DQ37	235	V <sub>SS</sub>	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	V <sub>SS</sub>	105	CB3/NC	171	V <sub>SS</sub>	237	DQ56	40	V <sub>SS</sub>	106	V <sub>SS</sub>	172	V <sub>SS</sub>	238	V <sub>SS</sub>
41	DQ10	107	V <sub>SS</sub>	173	DQ33	239	V <sub>SS</sub>	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	V <sub>SS</sub>	109	CKE0	175	V <sub>SS</sub>	241	DM7_n/ DBI7_n	44	V <sub>SS</sub>	110	CKE1	176	V <sub>SS</sub>	242	DQS7_t
45	DQ21	111	V <sub>DD</sub>	177	DQS4_c	243	V <sub>SS</sub>	46	DQ20	112	V <sub>DD</sub>	178	DM4_n/ DBI4_n	244	V <sub>SS</sub>
47	V <sub>SS</sub>	113	BG1	179	DQS4_t	245	DQ62	48	V <sub>SS</sub>	114	ACT_n	180	V <sub>SS</sub>	246	DQ63
49	DQ17	115	BG0	181	V <sub>SS</sub>	247	V <sub>SS</sub>	50	DQ16	116	ALERT_n	182	DQ39	248	V <sub>SS</sub>
51	V <sub>SS</sub>	117	V <sub>DD</sub>	183	DQ38	249	DQ58	52	V <sub>SS</sub>	118	V <sub>DD</sub>	184	V <sub>SS</sub>	250	DQ59
53	DQS2_c	119	A12	185	V <sub>SS</sub>	251	V <sub>SS</sub>	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	V <sub>SS</sub>
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	V <sub>SS</sub>	122	A7	188	V <sub>SS</sub>	254	SDA
57	V <sub>SS</sub>	123	V <sub>DD</sub>	189	V <sub>SS</sub>	255	V <sub>DDSPS</sub>	58	DQ22	124	V <sub>DD</sub>	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	V <sub>pp</sub>	60	V <sub>SS</sub>	126	A5	192	V <sub>SS</sub>	258	V <sub>TT</sub>
61	V <sub>SS</sub>	127	A6	193	V <sub>SS</sub>	259	V <sub>pp</sub>	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	V <sub>DD</sub>	195	DQ40	—	—	64	V <sub>SS</sub>	130	V <sub>DD</sub>	196	V <sub>SS</sub>	—	—
65	V <sub>SS</sub>	131	A3	197	V <sub>SS</sub>	—	—	66	DQ28	132	A2	198	DQS5_c	—	—

## Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A17 <sup>1</sup>	SDRAM address bus	SCL	I <sup>2</sup> C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I <sup>2</sup> C serial bus line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0-SA2	I <sup>2</sup> C slave address select for SPD-TSE
RAS <sub>n</sub> <sup>2</sup>	SDRAM row address strobe	PARITY	SDRAM parity input
CAS <sub>n</sub> <sup>3</sup>	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE <sub>n</sub> <sup>4</sup>	SDRAM write enable	C0, C1, C2	Chip ID lines
CS0 <sub>n</sub> , CS1 <sub>n</sub>	DIMM Rank Select Lines	12V	Optional power Supply on socket but not used on UDIMM
CKE0, CEK1	SDRAM clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines input	VSS	Power supply return (ground)
ACT <sub>n</sub>	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT <sub>n</sub>	SDRAM ALERT <sub>n</sub> output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0 <sub>t</sub> -TDQS8 <sub>t</sub> TDQS0 <sub>c</sub> -TDQS8 <sub>c</sub>	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0 <sub>t</sub> -DQS8 <sub>t</sub>	SDRAM data strobes (positive line of differential pair)		
DQS0 <sub>c</sub> -DQS8 <sub>c</sub>	SDRAM data strobes (negative line of differential pair)	RESET <sub>n</sub>	Set DRAMs to a Known State
DM0 <sub>n</sub> -DM8 <sub>n</sub> , DBI0 <sub>n</sub> -DBI8 <sub>n</sub>	SDRAM data masks/data bus inersion (x8-based x72 DIMMs)	EVENT <sub>n</sub>	SPD signals a thermal event has occurred
CK0 <sub>t</sub> , CK1 <sub>t</sub>	SDRAM clock (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0 <sub>c</sub> , CK1 <sub>c</sub>	SDRAM clock (negative line of differential pair)	RFU	Reserved for future use

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs, this connection pin is NC.
2. RAS<sub>n</sub> is a multiplexed function with A16.
3. CAS<sub>n</sub> is a multiplexed function with A15.
4. WE<sub>n</sub> is a multiplexed function with A14.

## Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
$T_{OPR}$	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,3

Notes 1. Operating Temperature  $T_{OPER}$  is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

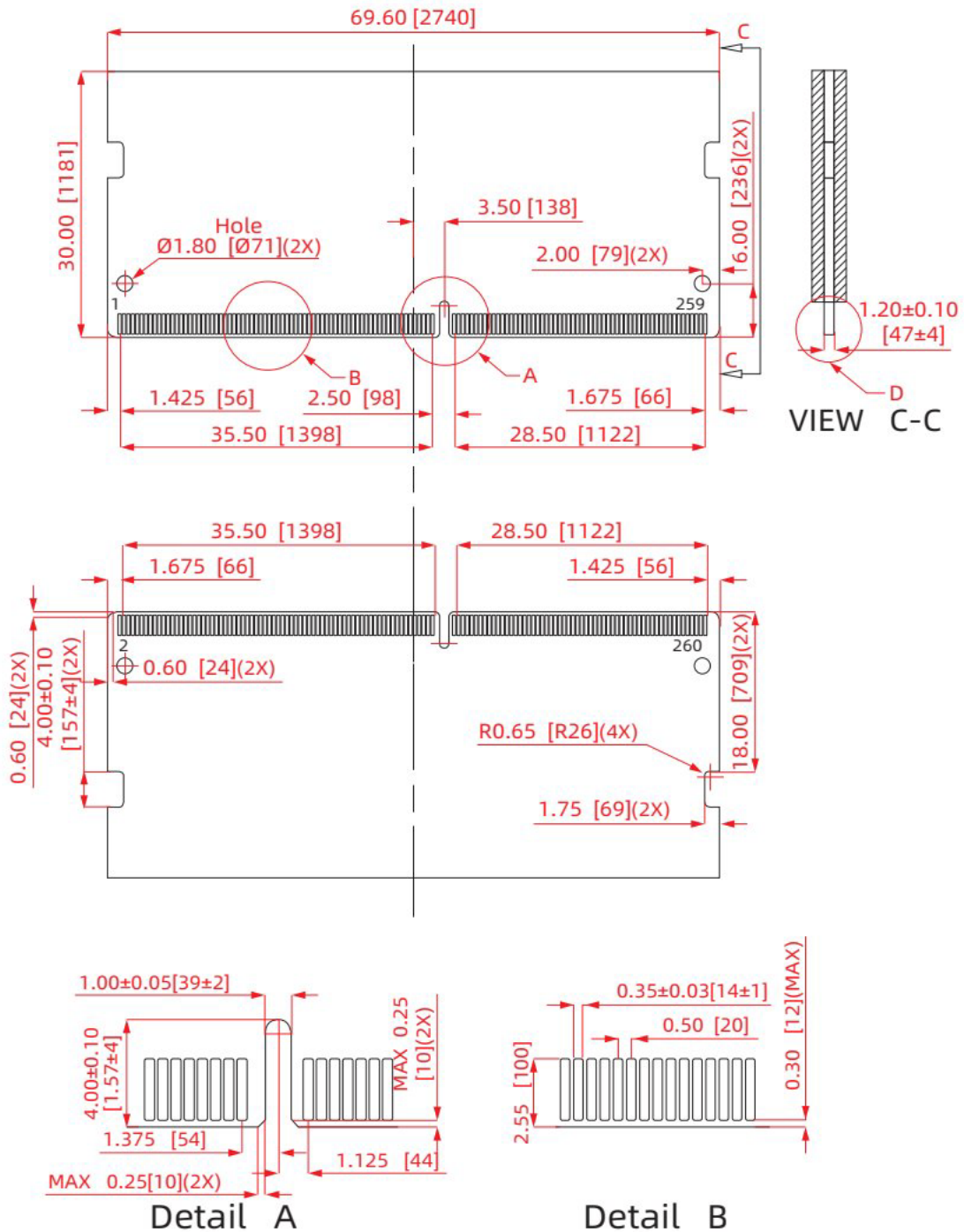
Notes 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

Notes 3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

- a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval  $t_{REFI}$  to 3.9  $\mu$ s. It is also possible to specify a component with 1X refresh ( $t_{REFI}$  to 7.8 $\mu$ s) in the Extended Temperature Range. Please refer to DIMM SPD for option availability.
- b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Follow JEDEC specification.

## Physical Dimensions



Note:  
All dimensions are in millimeters[mils] and should be kept within a tolerance of  $\pm 0.15$  [6], unless otherwise specified.

※Above Picture is for reference only!

Units: Millimeters