GENERAL DESCRIPTION

This chapter gives an overview of the 204-pin SO DDR3 Dual-In-Line memory modules product family and describes its main characteristics.

FEATURES

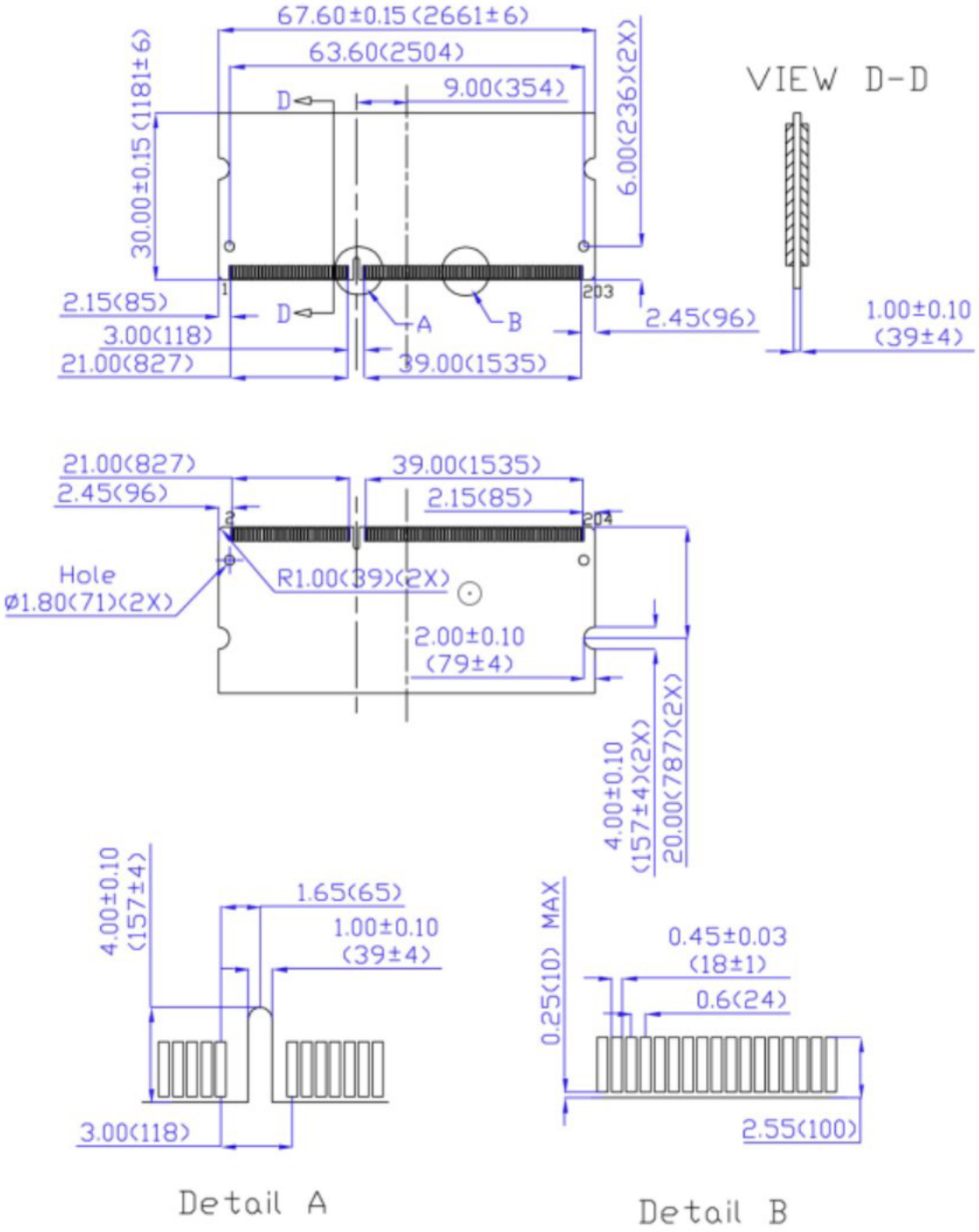
- VDD=VDDQ=1.35V +/- 0.06V
- VPP = 3.0V to 3.6V
- Fully differential clock inputs（CK,CK）operation
- Differential Data Strobe（DQS,DQS）
- On chip DLL align DQ,DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle

  -7.8 μs at 0°C~85°C
- JEDEC standard 78ball FBGA (x4 / x8)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- This product in compliance with the RoHS directive

Information for Compliant Products

Product Type	Compliance Code	Description
IND-ID3N10SP08X	8GB DDR3-1066 7/7/7	1 Ran, Non-ECC
IND-ID3N13SP08X	8GB DDR3-1333 9/9/9	1 Ran, Non-ECC
IND-ID3N16SP08X	8GB DDR3-1600 11/11/11	1 Ran, Non-ECC
IND-ID3N18SP08X	8GB DDR3-1866 13/13/13	1 Ran, Non-ECC

Physical Dimensions



Note:
All dimensions are in millimeters[mils] and should be
kept wihtin a tolerance of ±0.15[6], unless otherwise specified.
※Above Picture is for reference only!

Units: Millimeters