GENERAL DESCRIPTION

This chapter gives an overview of the 262-pin SO-DDR5 memory modules product family and describes its main characteristics.

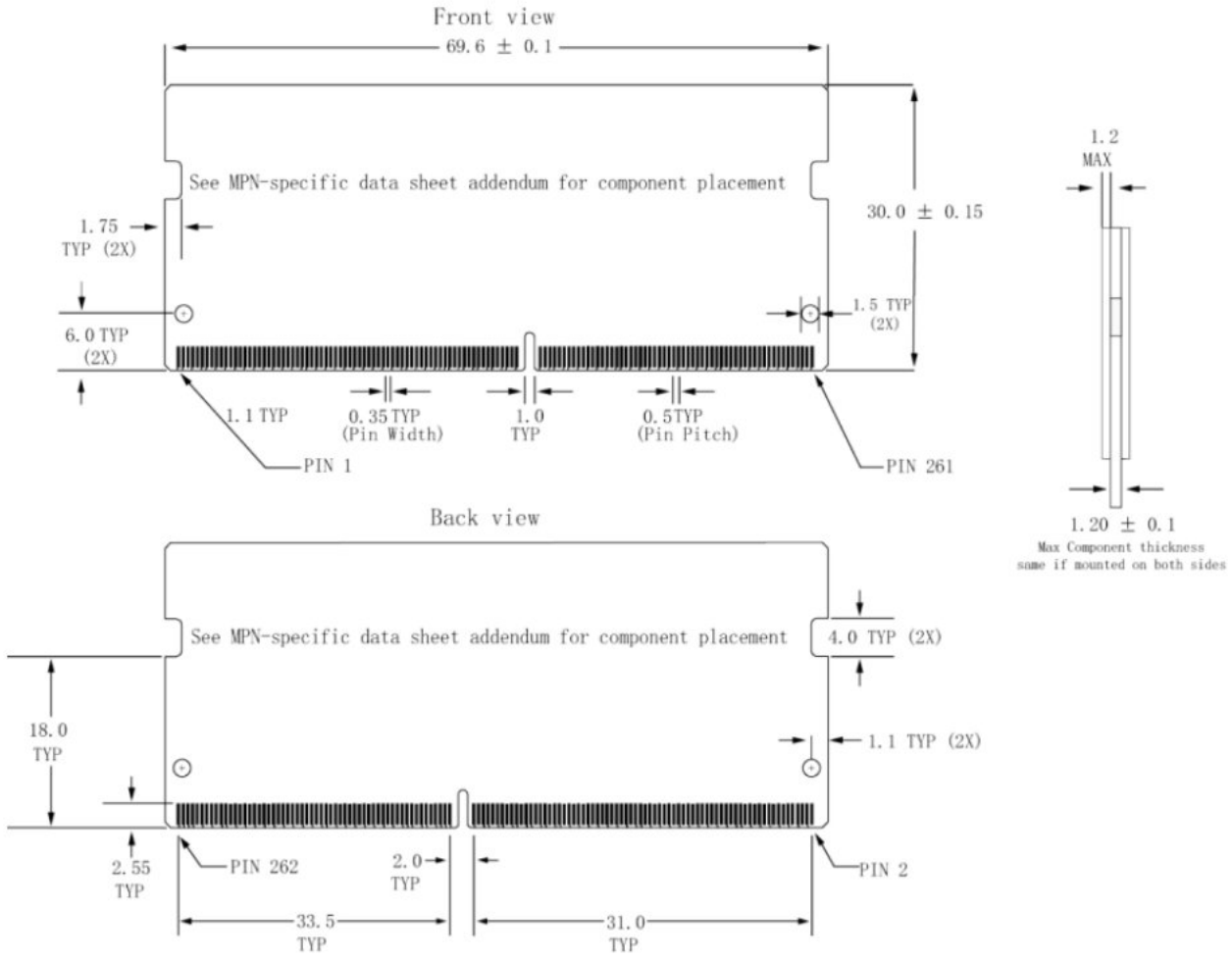
FEATURES

- VDD=VDDQ=1.1V +/- 0.06V
- VPP = 1.8V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C – 32ms, 8192-cycle refresh up to 85°C – 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2n mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- JEDEC JESD-79.5 compliant

Information for Compliant Products

Product Type	Compliance Code
IND-ID5N48SP32X	32GB DDR5-4800 40/40/40/82
IND-ID5N52SP32X	32GB DDR5-5200 42/42/42/83
IND-ID5N56SP32X	32GB DDR5-5600 46/46/46/90
IND-ID5N60SP32X	32GB DDR5-6000 38/46/46/90

Physical Dimensions



Note:
All dimensions are in millimeters[mils] and should be
kept wihtin a tolerance of ±0.15[6], unless otherwise specified.

※Above Picture is for reference only!

Units: Millimeters