GENERAL DESCRIPTION

This chapter gives an overview of the 260-pin SO DDR4 Dual-In-Line memory modules product family and describes its main characteristics.

FEATURES

- VDD=VDDQ=1.2V +/- 0.06V
- VPP = 2.5V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 85°C

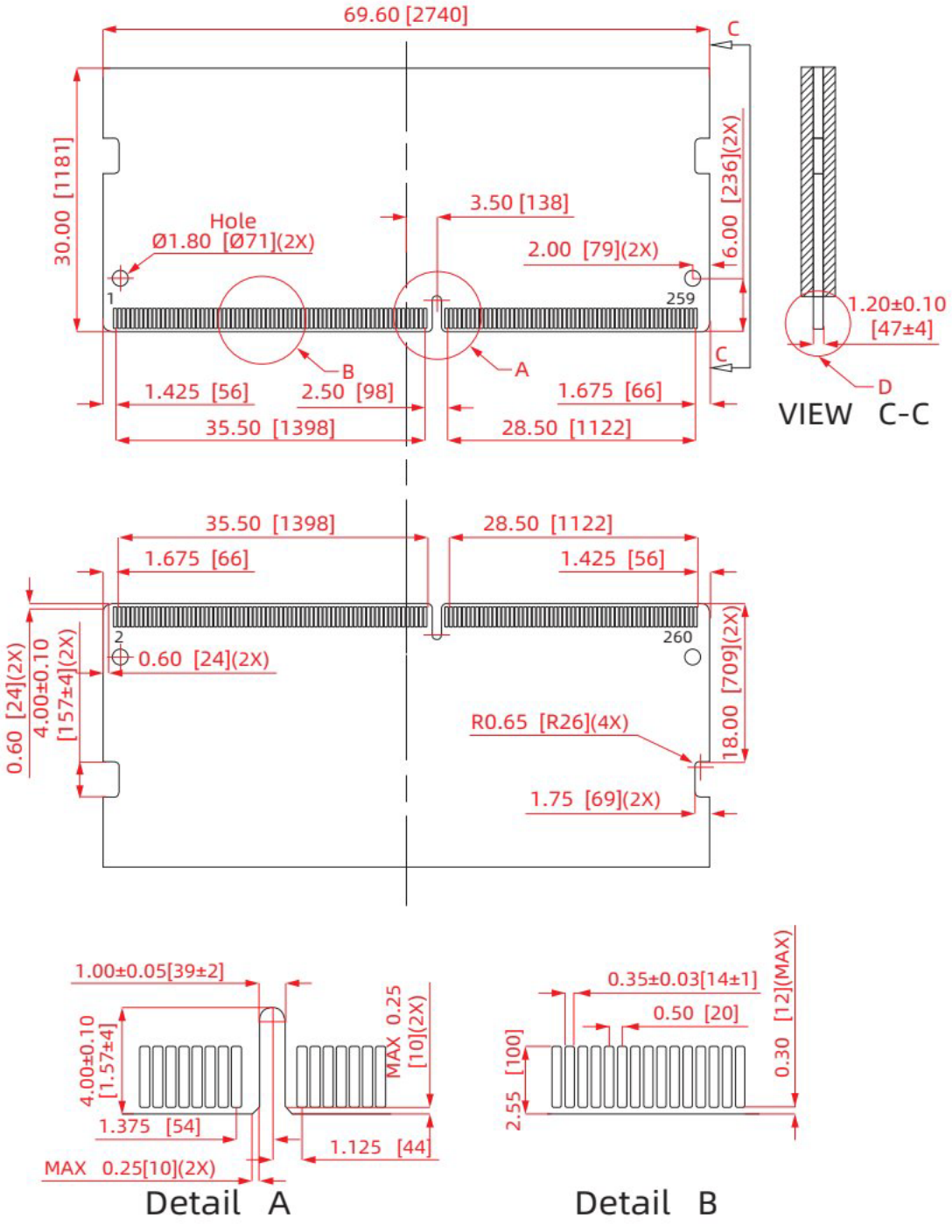
– 64ms, 8192-cycle refresh at 0°C to 85°C

- JEDEC standard 78ball FBGA
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Post package repair (PPR) and soft post package repair (sPPR) modes • JEDEC JESD-79-4 compliant

Information for Compliant Products

Product Type	Compliance Code	Description
IND-ID4N21SP32X	32GB DDR4-2133 15/15/15	1 Ran, Non-ECC
IND-ID4N24SP32X	32GB DDR4-2400 17/17/17	1 Ran, Non-ECC
IND-ID4N26SP32X	32GB DDR4-2666 19/19/19	1 Ran, Non-ECC
IND-ID4N29SP32X	32GB DDR4-2933 21/21/21	1 Ran, Non-ECC
IND-ID4N32SP32X	32GB DDR4-3200 22/22/22	1 Ran, Non-ECC

Physical Dimensions



Note:
All dimensions are in millimeters[mils] and should be kept wihtin a tolerance of ±0.15[6], unless otherwise specified.

※Above Picture is for reference only!

Units: Millimeters