

GENERAL DESCRIPTION

This chapter gives an overview of the 288-pin DDR5 memory modules product family and describes its main characteristics.

FEATURES

- VDD=VDDQ=1.1V or 1.25V+/- 0.06V
- VPP = 1.8V, -125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C – 32ms, 8192-cycle refresh up to 85°C – 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2n mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- JEDEC JESD-79.5 compliant

Information for Compliant Products

Product Type	Compliance Code
IND-ID5P48SP16X	16GB DDR5-4800 40/40/40/82
IND-ID5P52SP16X	16GB DDR5-5200 42/42/42/83
IND-ID5P56SP16X	16GB DDR5-5600 46/46/46/90
IND-ID5P60SP16X	16GB DDR5-6000 38/46/46/90
IND-ID5P64SP16X	16GB DDR5-6400 38/50/50/90

Pinout

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V _{SS}	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V _{SS}
2	RFU	38	V _{SS}	74	V _{SS}	110	DQ5_B	146	VIN_BULK	182	V _{SS}	218	V _{SS}	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	V _{SS}	147	PWR_GOOD	183	DQ23_A	219	RFU	255	V _{SS}
4	HSCL	40	V _{SS}	76	RFU	112	DQ8_B	148	HSA	184	V _{SS}	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	V _{SS}	113	V _{SS}	149	RFU	185	DQ26_A	221	V _{SS}	257	V _{SS}
6	V _{SS}	42	V _{SS}	78	CK0_B_t	114	DQ9_B	150	V _{SS}	186	V _{SS}	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V _{SS}	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V _{SS}
8	V _{SS}	44	V _{SS}	80	V _{SS}	116	DM1_B_n	152	RFU	188	V _{SS}	224	V _{SS}	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	V _{SS}	153	V _{SS}	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	V _{SS}	46	V _{SS}	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	V _{SS}
11	DQ1_A	47	DQ28_A	83	V _{SS}	119	V _{SS}	155	V _{SS}	191	V _{SS}	227	V _{SS}	263	DQ14_B
12	V _{SS}	48	V _{SS}	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	V _{SS}
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	V _{SS}	157	V _{SS}	193	V _{SS}	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	V _{SS}	86	V _{SS}	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	V _{SS}	266	V _{SS}
15	V _{SS}	51	CB0_A	87	CA6_B	123	V _{SS}	159	V _{SS}	195	V _{SS}	231	CA7_B	267	DQ18_B
16	DQ4_A	52	V _{SS}	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	V _{SS}
17	V _{SS}	53	CB1_A	89	V _{SS}	125	V _{SS}	161	V _{SS}	197	V _{SS}	233	V _{SS}	269	DQ19_B
18	DQ5_A	54	V _{SS}	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	V _{SS}
19	V _{SS}	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	V _{SS}	199	V _{SS}	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	V _{SS}	128	V _{SS}	164	DQ10_A	200	ALERT_n	236	V _{SS}	272	V _{SS}
21	V _{SS}	57	V _{SS}	93	CS0_B_n	129	DQ20_B	165	V _{SS}	201	V _{SS}	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	V _{SS}	130	V _{SS}	166	DQ11_A	202	CS1_A_n	238	V _{SS}	274	V _{SS}
23	V _{SS}	59	V _{SS}	95	RESET_n	131	DQ21_B	167	V _{SS}	203	V _{SS}	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	V _{SS}	132	V _{SS}	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	V _{SS}
25	V _{SS}	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	V _{SS}	277	DQ26_B
26	DQ12_A	62	V _{SS}	98	V _{SS}	134	V _{SS}	170	V _{SS}	206	V _{SS}	242	CB2_B	278	V _{SS}
27	V _{SS}	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	V _{SS}	279	DQ27_B
28	DQ13_A	64	CA6_A	100	V _{SS}	136	V _{SS}	172	V _{SS}	208	CA7_A	244	CB3_B	280	V _{SS}
29	V _{SS}	65	V _{SS}	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	V _{SS}	245	V _{SS}	281	DQS3_B_c
30	DQ16_A	66	CA8_A	102	V _{SS}	138	V _{SS}	174	V _{SS}	210	CA9_A	246	DQ2_B	282	DQS3_B_t
31	V _{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	V _{SS}	283	V _{SS}
32	DQ17_A	68	V _{SS}	104	V _{SS}	140	V _{SS}	176	V _{SS}	212	V _{SS}	248	DQ3_B	284	DQ30_B
33	V _{SS}	69	CA12_A	105	DQS0_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	V _{SS}	285	V _{SS}
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	V _{SS}	178	V _{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQS2_A_t	71	V _{SS}	107	V _{SS}	143	RFU	179	DM2_A_n	215	V _{SS}	251	V _{SS}	287	V _{SS}
36	V _{SS}	72	CK0_A_t	108	DQ4_B	144	RFU	180	V _{SS}	216	CK1_A_t	252	DQ6_B	288	RFU

Pin Descriptions

Symbol	Type	I/O Level	Description
CK_t, CK_c	Input	V _{DDQ}	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:0]_A CA[12:0]_B	Input	V _{DDQ}	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands. The DDR5 component CA13 pin is strapped (connected) to either V _{SS} or V _{DDQ} depending on the strapped state of MIR. Refer to Address Mapping to DRAM (page 8) for detail.
CS[1:0]_A CS[1:0]_B	Input	V _{DDQ}	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V _{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V _{DDQ} .
ALERT_n	Output	V _{DDQ}	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V _{DDQ} on the system board.
RESET_n	CMOS Input	V _{DDQ}	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V _{DDQ} .
PWR_GOOD	Input/ Output	V _{DDQ}	Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.8V or VOUT_1.0V	Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.

Symbol	Type	I/O Level	Description
HSDA	Input/Output	VOUT_1.8V or VOUT_1.0V	Host Sideband Bus Data: I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
DQ[31:0]_A DQ[31:0]_B	Input/Output	V _{DDQ}	Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0–DQ3 may indicate the internal V ^{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[3:0]_A CB[3:0]_B	Input/Output	V _{DDQ}	ECC Check Bits Input/Output: Bidirectional data bus.
DQS[4:0]_A_t DQS[4:0]_B_t DQS[4:0]_A_c DQS[4:0]_B_c	Input/Output	V _{DDQ}	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DM[3:0]_A_n DM[3:0]_B_n	Input	V _{DDQ}	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5] = 1.
VIN_BULK	Supply		External Power Supply: 5V, 4.25V (min), 5.5V (max)
PWR_EN	Input		PMIC Enable: When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
V _{SS}	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			No connect: No internal electrical connection is present.
NF			No function: May have internal connection present, but has no function.

Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2,3
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,2,3,4

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

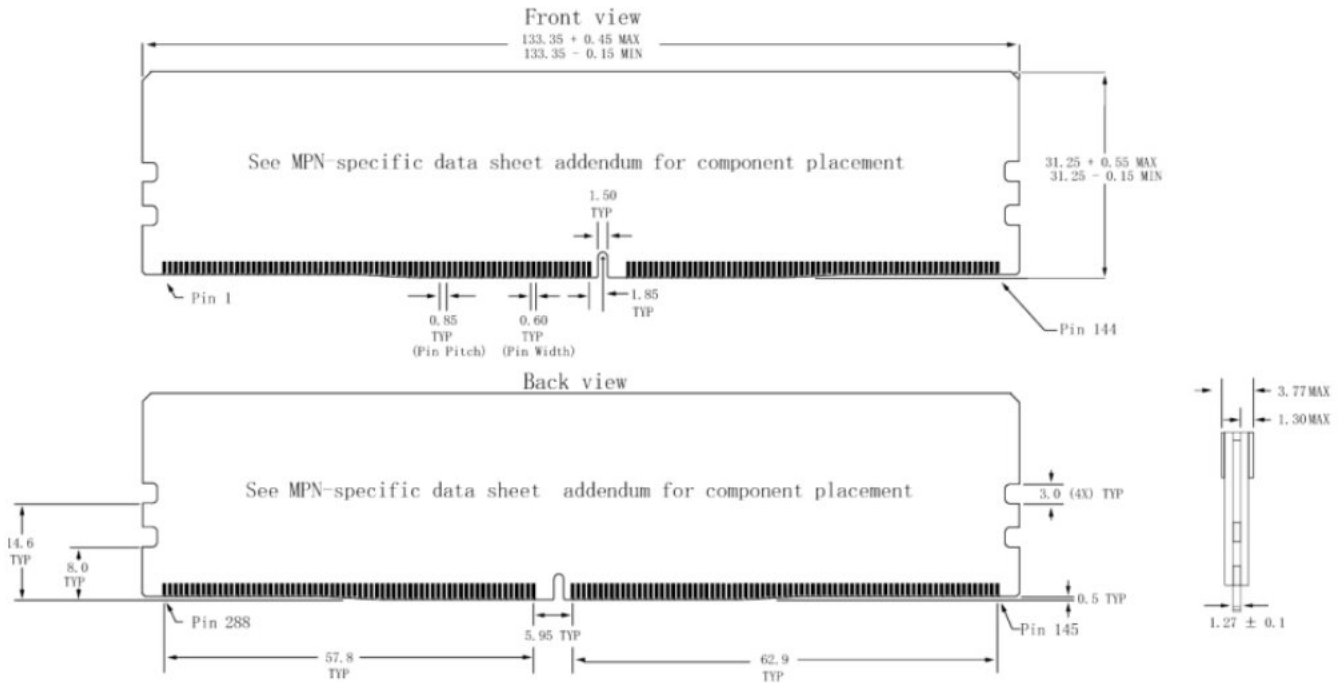
NOTE 2 The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85°C under all operating conditions.

NOTE 3 Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: $[T_{OPER} - (2.5^{\circ}\text{C} \times \log_2 N)]$, where N is the number of the stacked dies.

NOTE 4 Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

- Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range. Please refer to supplier's datasheet and/or the DIMM SPD for option availability.
- If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0b and MR2 A7=1b) or enable the optional Auto Self-Refresh mode (MR2 A6=1b and MR2 A7=0b). Please refer to the supplier's datasheet and/or the DIMM SPD for Auto Self-Refresh option availability. Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

Physical Dimensions



Note:
 All dimensions are in millimeters[mils] and should be kept within a tolerance of $\pm 0.15[6]$, unless otherwise specified.
 ※Above Picture is for reference only!

Units: Millimeters