GENERAL DESCRIPTION

This chapter gives an overview of the 262-pin SO-DDR5 memory modules product family and describes its main characteristics.

FEATURES

- VDD=VDDQ=1.1V +/- 0.06V
- VPP = 1.8V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C – 32ms, 8192-cycle refresh up to 85°C – 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2n mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- JEDEC JESD-79.5 compliant

Information for Compliant Products

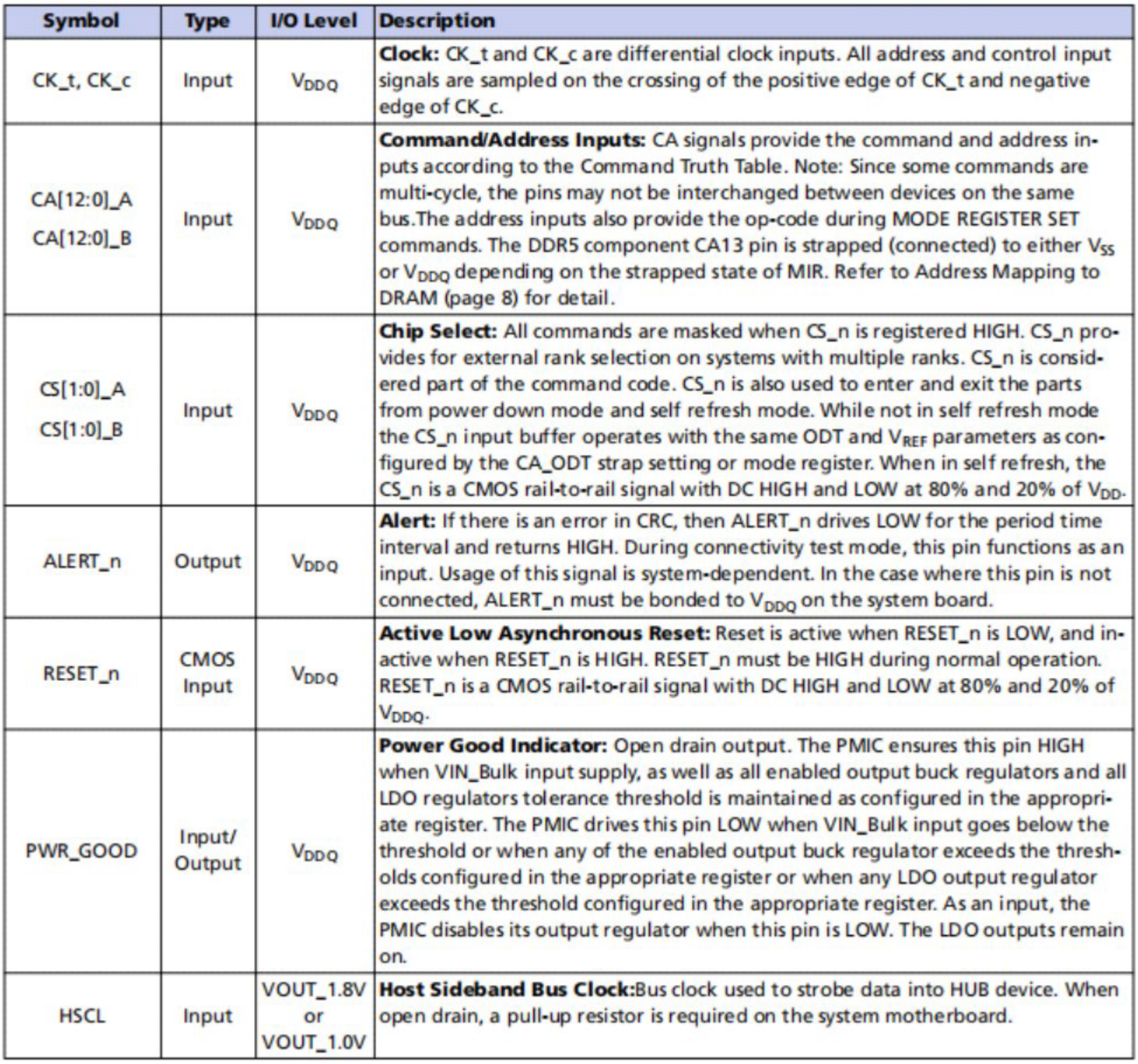
Product Type	Compliance Code
IND-ID5N48SP16X	16GB DDR5-4800 40/40/40/82
IND-ID5N52SP16X	16GB DDR5-5200 42/42/42/83
IND-ID5N56SP16X	16GB DDR5-5600 46/46/46/90
IND-ID5N60SP16X	16GB DDR5-6000 38/46/46/90

Pinout

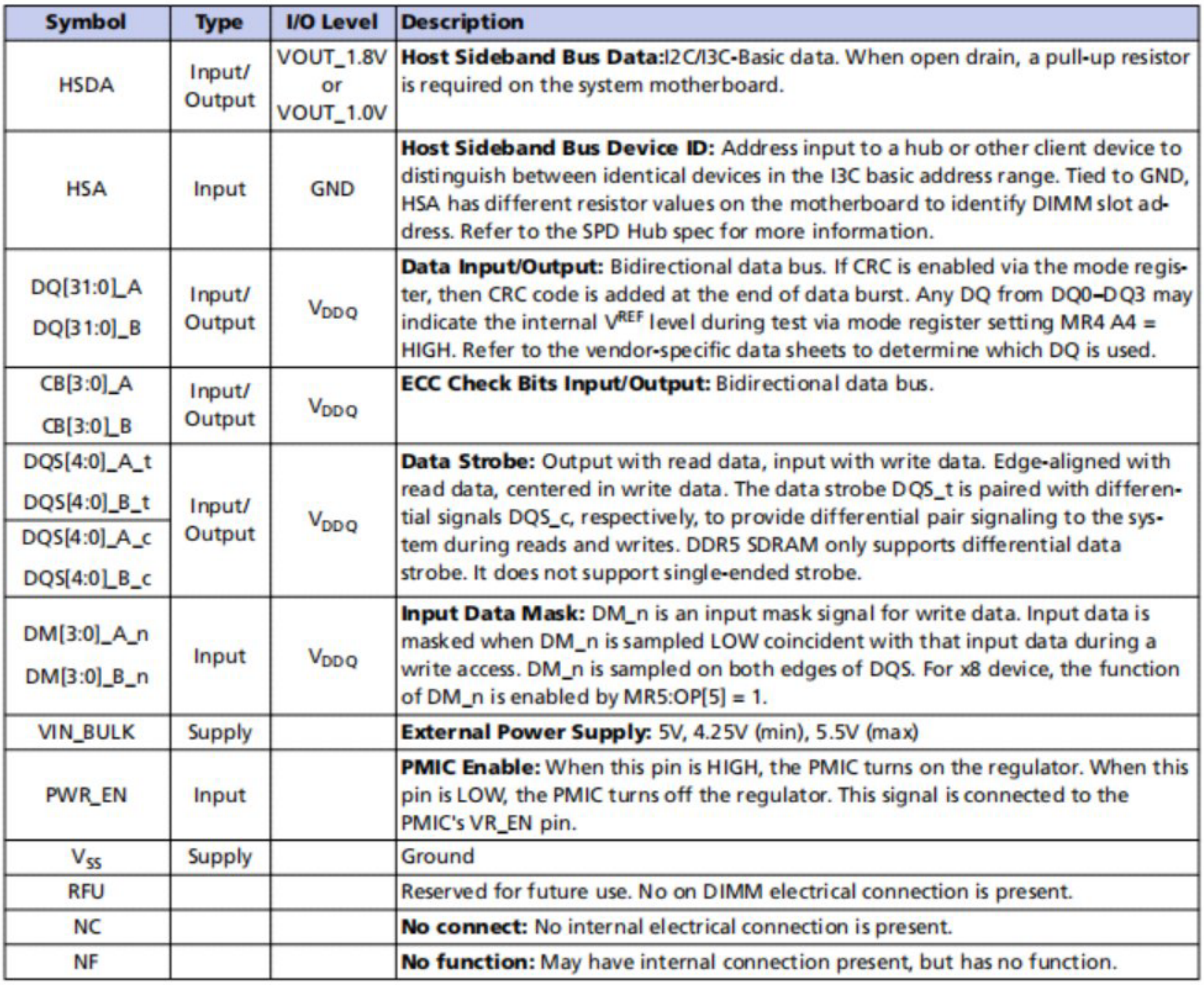
262-Pin DDR5 SODIMM Front					
Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	89	V_{SS}	175	CB3_B
3	VIN_BULK	91	DQ30_A	177	V_{SS}
5	RFU	93	V_{SS}	179	DQ0_B
7	PWR_GOOD	95	CB0_A	181	V_{SS}
9	V_{SS}	97	V_{SS}	183	DQ2_B
11	DQ0_A	99	CB2_A	185	V_{SS}
13	V_{SS}	101	V_{SS}	187	DM0_B_n
15	DQ2_A	103	CB3_A	189	V_{SS}
17	V_{SS}	105	V_{SS}	191	DQ4_B
19	DM0_A_n	107	CA0_A	193	V_{SS}
21	V_{SS}	109	CA1_A	195	DQ6_B
23	DQ4_A	111	V_{SS}	197	V_{SS}
25	V_{SS}	113	CA2_A	199	DQ8_B
27	DQ6_A	115	CA4_A	201	V_{SS}
29	V_{SS}	117	V_{SS}	203	DQ10_B
31	DQ8_A	119	CA6_A	205	V_{SS}
33	V_{SS}	121	CA8_A	207	DQS1_B_c
35	DQ10_A	123	V_{SS}	209	DQS1_B_t
37	V_{SS}	125	CA10_A	211	V_{SS}
39	DQS1_A_c	KEY		213	DQ12_B
41	DQS1_A_t	127	CA12_A	215	V_{SS}
43	V_{SS}	129	V_{SS}	217	DQ14_B
45	DQ12_A	131	CK0_A_t	219	V_{SS}
47	V_{SS}	133	CK0_A_c	221	DQ16_B
49	DQ14_A	135	V_{SS}	223	V_{SS}
51	V_{SS}	137	CK0_B_t	225	DQ18_B
53	DQ16_A	139	CK0_B_c	227	V_{SS}
55	V_{SS}	141	V_{SS}	229	DM2_B_n
57	DQ18_A	143	RFU	231	V_{SS}
59	V_{SS}	145	CA11_B	233	DQ20_B
61	DM2_A_n	147	V_{SS}	235	V_{SS}
63	V_{SS}	149	CA9_B	237	DQ22_B
65	DQ20_A	151	CA7_B	239	V_{SS}
67	V_{SS}	153	V_{SS}	241	DQ24_B
69	DQ22_A	155	CA5_B	243	V_{SS}
71	V_{SS}	157	CA3_B	245	DQ26_B
73	DQ24_A	159	V_{SS}	247	V_{SS}
75	V_{SS}	161	CS0_B_n	249	DQS3_B_c
77	DQ26_A	163	RESET_n	251	DQS3_B_t
79	V_{SS}	165	CS1_B_n	253	V_{SS}
81	DQS3_A_c	167	V_{SS}	255	DQ28_B
83	DQS3_A_t	169	DQS4_B_c	257	V_{SS}
85	V_{SS}	171	DQS4_B_t	259	DQ30_B
87	DQ28_A	173	V_{SS}	261	V_{SS}

262-Pin DDR5 SODIMM Back					
Pin	Symbol	Pin	Symbol	Pin	Symbol
2	HSA	90	V_{SS}	176	CB2_B
4	HSCL	92	DQ31_A	178	V_{SS}
6	HSDA	94	V_{SS}	180	DQ1_B
8	PWR_EN	96	CB1_A	182	V_{SS}
10	V_{SS}	98	V_{SS}	184	DQ3_B
12	DQ1_A	100	DQS4_A_c	186	V_{SS}
14	V_{SS}	102	DQS4_A_t	188	DQS0_B_c
16	DQ3_A	104	V_{SS}	190	DQS0_B_t
18	V_{SS}	106	CS0_A_n	192	V_{SS}
20	DQS0_A_	108	ALERT_n	194	DQ5_B
22	DQS0_A_	110	CS1_A_n	196	V_{SS}
24	V_{SS}	112	V_{SS}	198	DQ7_B
26	DQ5_A	114	CA3_A	200	V_{SS}
28	V_{SS}	116	CA5_A	202	DQ9_B
30	DQ7_A	118	V_{SS}	204	V_{SS}
32	V_{SS}	120	CA7_A	206	DQ11_B
34	DQ09_A	122	CA9_A	208	V_{SS}
36	V_{SS}	124	V_{SS}	210	DM1_B_n
38	DQ11_A	126	CA11_A	212	V_{SS}
40	V_{SS}	KEY		214	DQ13_B
42	DM1_A_n	128	RFU	216	V_{SS}
44	V_{SS}	130	V_{SS}	218	DQ15_B
46	DQ13_A	132	CK1_A_t	220	V_{SS}
48	V_{SS}	134	CK1_A_c	222	DQ17_B
50	DQ15_A	136	V_{SS}	224	V_{SS}
52	V_{SS}	138	CK1_B_t	226	DQ19_B
54	DQ17_A	140	CK1_B_c	228	V_{SS}
56	V_{SS}	142	V_{SS}	230	DQS2_B_c
58	DQ19_A	144	CA12_B	232	DQS2_B_t
60	V_{SS}	146	CA10_B	234	V_{SS}
62	DQS2_A_c	148	V_{SS}	236	DQ21_B
64	DQS2_A_t	150	CA8_B	238	V_{SS}
66	V_{SS}	152	CA6_B	240	DQ23_B
68	DQ21_A	154	V_{SS}	242	V_{SS}
70	V_{SS}	156	CA4_B	244	DQ25_B
72	DQ23_A	158	CA2_B	246	V_{SS}
74	V_{SS}	160	V_{SS}	248	DQ27_B
76	DQ25_A	162	CA1_B	250	V_{SS}
78	V_{SS}	164	CA0_B	252	DM3_B_n
80	DQ27_A	166	V_{SS}	254	V_{SS}
82	V_{SS}	168	CB0_B	256	DQ29_B
84	DM3_A_n	170	V_{SS}	258	V_{SS}
86	V_{SS}	172	CB1_B	260	DQ31_B
88	DQ29_A	174	V_{SS}	262	V_{SS}

Pin Descriptions



Symbol	Type	I/O Level	Description
CK_t, CK_c	Input	V_{DDQ}	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:0]_A CA[12:0]_B	Input	V_{DDQ}	**Command/Address Inputs:** CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.The address inputs also provide the op-code during MODE REGISTER SET commands. The DDR5 component CA13 pin is strapped (connected) to either V_{SS} or V_{DDQ} depending on the strapped state of MIR. Refer to Address Mapping to DRAM (page 8) for detail.
CS[1:0]_A CS[1:0]_B	Input	V_{DDQ}	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}.
ALERT_n	Output	V_{DDQ}	**Alert:** If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
RESET_n	CMOS Input	V_{DDQ}	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ}.
PWR_GOOD	Input/ Output	V_{DDQ}	**Power Good Indicator:** Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Clock:**Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.



Symbol	Type	I/O Level	Description
HSDA	Input/ Output	VOUT_1.8V or VOUT_1.0V	**Host Sideband Bus Data:**I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	**Host Sideband Bus Device ID:** Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.
DQ[31:0]_A DQ[31:0]_B	Input/ Output	V_{DDQ}	**Data Input/Output:** Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0–DQ3 may indicate the internal V^{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[3:0]_A CB[3:0]_B	Input/ Output	V_{DDQ}	**ECC Check Bits Input/Output:** Bidirectional data bus.
DQS[4:0]_A_t DQS[4:0]_B_t DQS[4:0]_A_c DQS[4:0]_B_c	Input/ Output	V_{DDQ}	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DM[3:0]_A_n DM[3:0]_B_n	Input	V_{DDQ}	**Input Data Mask:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5] = 1.
VIN_BULK	Supply		**External Power Supply:** 5V, 4.25V (min), 5.5V (max)
PWR_EN	Input		**PMIC Enable:** When this pin is HIGH, the PMIC turns on the regulator. When this pin is LOW, the PMIC turns off the regulator. This signal is connected to the PMIC's VR_EN pin.
V_{SS}	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			**No connect:** No internal electrical connection is present.
NF			**No function:** May have internal connection present, but has no function.

Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2,3
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,2,3,4

NOTE 1 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 2 The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85°C under all operating conditions.

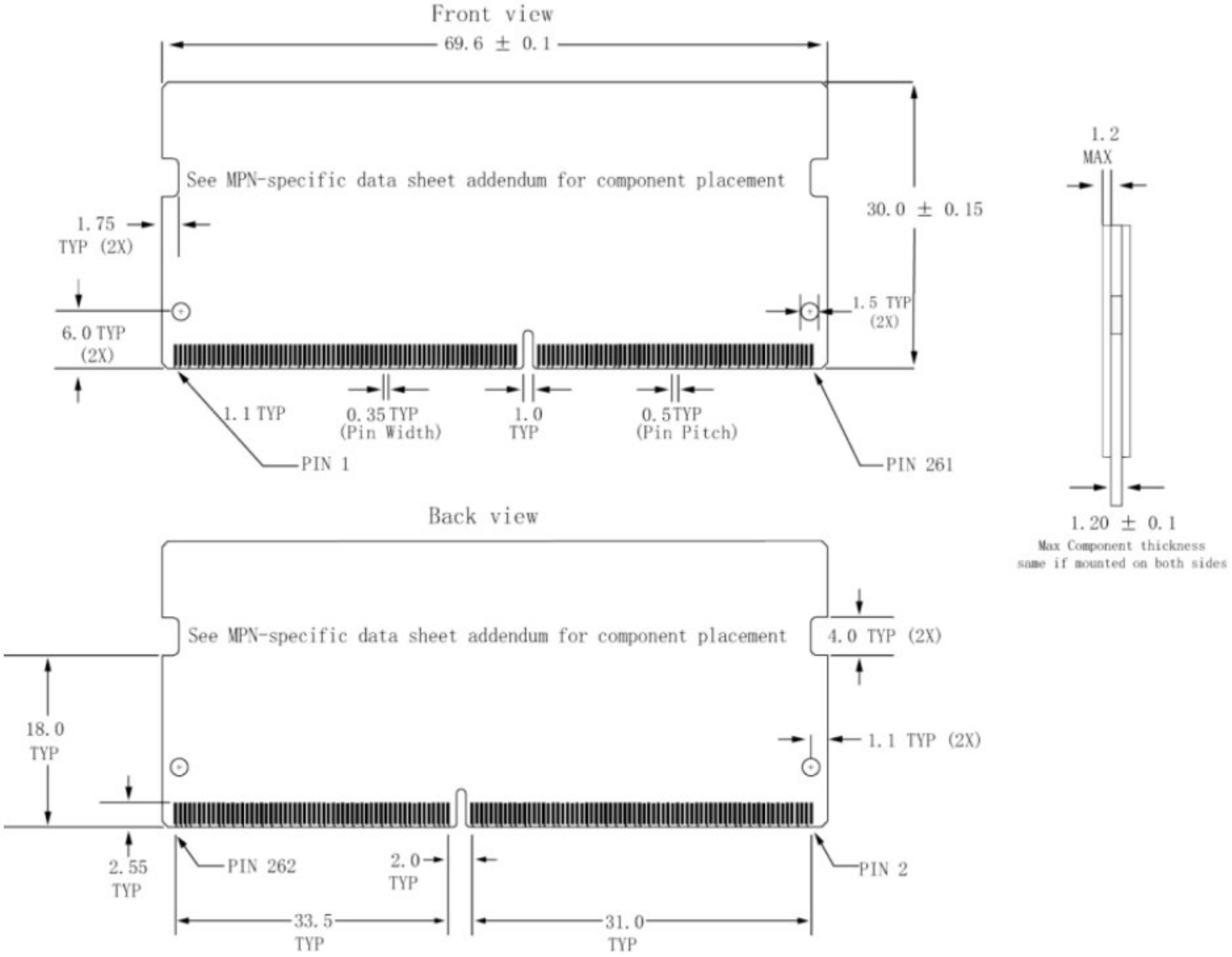
NOTE 3 Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [T_{OPER} – (2.5°C × $\log_2 N$)], where N is the number of the stacked dies.

NOTE 4 Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range. Please refer to supplier's datasheet and/or the DIMM SPD for option availability.

b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0b and MR2 A7=1b) or enable the optional Auto Self-Refresh mode (MR2 A6=1b and MR2 A7=0b). Please refer to the supplier's datasheet and/or the DIMM SPD for Auto Self-Refresh option availability. Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

Physical Dimensions



Note:
All dimensions are in millimeters[mils] and should be
kept wihtin a tolerance of ±0.15[6]，unless otherwise specified.

※Above Picture is for reference only!

Units：Millimeters