GENERAL DESCRIPTION

This chapter gives an overview of the 288–pin DDR4 Dual-In-Line memory modules product family and describes its main characteristics.

FEATURES

- VDD=VDDQ=1.2V +/- 0.06V
- VPP = 2.5V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 85°C

– 64ms, 8192-cycle refresh at 0°C to 85°C

- JEDEC standard 78ball FBGA
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination(ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Post package repair (PPR) and soft post package repair (sPPR) modes • JEDEC JESD-79-4 compliant

Information for Compliant Products

Product Type	Compliance Code	Description
IND-ID4P21SP16X	16GB DDR4-2133 15/15/15	1 Ran, Non-ECC
IND-ID4P24SP16X	16GB DDR4-2400 17/17/17	1 Ran, Non-ECC
IND-ID4P26SP16X	16GB DDR4-2666 19/19/19	1 Ran, Non-ECC
IND-ID4P29SP16X	16GB DDR4-2933 21/21/21	1 Ran, Non-ECC
IND-ID4P32SP16X	16GB DDR4-3200 22/22/22	1 Ran, Non-ECC
IND-ID4P36SP16X	16GB DDR4-3600 22/22/22	1 Ran, Non-ECC

Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
1	12V	145	12V	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	DQS9_t, DM0_n, DBI0_n, TDQS9_t	151	VSS	78	EVENT_n	222	PARITY
8	DQS9_c, TDQS9_c	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	S0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	Save_n,NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DQS10_t, DM1_n, DBI1_n, TDQS10_t	162	VSS	89	S1_n	233	VDD
19	DQS10_c, TDQS10_c	163	DQS1_c	90	VDD	234	A17, NC
20	VSS	164	DQS1_t	91	ODT1	235	C[2], NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	S2_n, C[0]	237	S3_n, C[1]
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	DQS13_t, DM4_n, DBI4_n, TDQS13_t	243	VSS
29	DQS11_t, DM2_n, DBI2_n, TDQS11_t	173	VSS	100	DQS13_c, TDQS13_c	244	DQS4_c

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
30	DQS11_c, TDQS11_c	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	DQS14_t, DM5_n, DBI5_n, TDQS14_t	254	VSS
40	DQS12_t, DM3_n, DBI3_n, TDQS12_t	184	VSS	111	DQS14_c, TDQS14_c	255	DQS5_C
41	DQS12_c, TDQS12_c	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4,NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5,NC	119	DQ48	263	VSS
49	CB0,NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1,NC	121	DQS15_t, DM6_n, DBI6_n, TDQS15_t	265	VSS
51	DQS17_t, DM8_n, DBI8_n, TDQS17_t	195	VSS	122	DQS15_c, TDQS15_c	266	DQS6_c
52	DQS17_c, TDQS17_c	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6,NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7,NC	126	DQ50	270	VSS
56	CB2,NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3,NC	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
61	VDD	205	RFU	132	DQS16_t, DM7_n, DBI7_n, TDQS16_t	276	VSS
62	ACT_n	206	VDD	133	DQS16_c, TDQS16_c	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

Pin Name	Description	Pin Name	Description
A0-A17[1]	SDRAM address bus	SCL	I^2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0-SA2	I^2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM I/OO and core power supply
WE_n[4]	SDRAM write enable	C0, C1, C2	Chip ID lines
CS0_n, CS1_n,	DIMM Rank Select Lines	12V	Optional power Supply on socket but not used on UDIMM
CKE0, CEK1	SDRAM clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs.		
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)		
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to a Known State
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inersion (x8-based x72 DIMMs)	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	SDRAM clock (positive line of differen-tial pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	SDRAM clock (positive line of differen-tial pair)	RFU	Reserved for future use

1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs, this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Normal Operating Temperature Range	0 ~ 85	°C	1,2
	Extended Temperature Range (Optional)	85 ~ 95	°C	1,3

Notes 1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

Notes 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

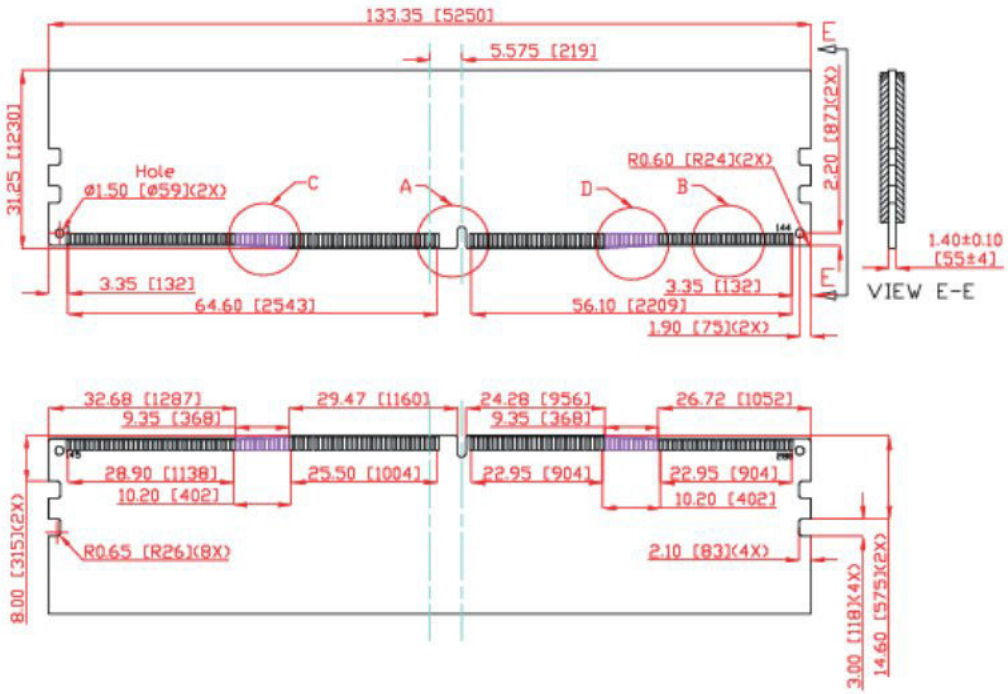
Notes 3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

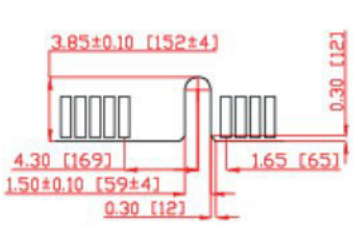
a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9 µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the Extended Temperature Range. Please refer to DIMM SPD for option availability.

b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

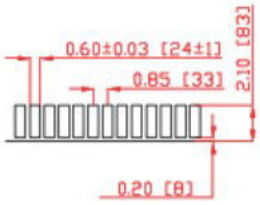
Follow JEDEC specification.

Module Dimensions





Detail A



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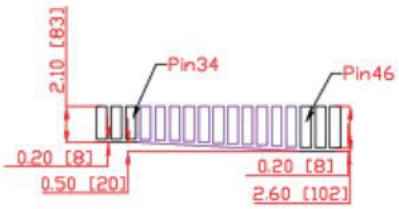

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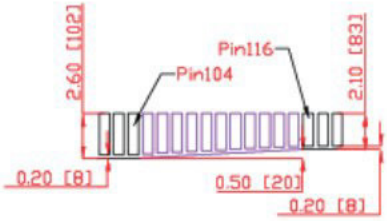

Detail D

Note:
All dimensions are in millimeters[mils] and should be
kept wihtin a tolerance of ±0.15 [6],unless otherwise specified.

※Above Picture is for reference only!

Units: Millimeters